Sampling Architectures

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Abstract — **In modern communication, sensor and signal processing systems digitization methods are gaining importance. They allow for building software configurable systems and provide better stability and reproducibility. The quest for new architectures in radio frequency front-ends is a clear consequence of the ever increasing number of different standards and the resulting task to provide a platform which covers as many standards as possible. The first part of this paper reviews multiband capable receiver architectures. These are limited to a few GHz yet. The second part proposes a novel architecture, which is capable of direct sampling of band-limited signals at frequencies beyond 10 GHz by means of an under-sampling technique.**

I. Introduction

Many applications of communication, sensor and signal processing systems would provide greater performance, if various standards could be handled with only one hardware device. One first step towards the aim of an ultimate software radio is the realization of a direct sampling receiver. Such a RF front-end being capable to digitize a wide range of frequencies together with a fast and powerful digital signal processing unit would allow for reception of any protocol, service or traffic information [1]. Moreover, several services could be received simultaneously, either in fully parallel or fast multiplexing mode. The input frequency and the channel bandwidth can be chosen in the receiver's digital part, fully independent of the used front-end.

The following section gives a short review of multiband capable receiver architectures. Then, a band-limited under-sampling architecture for 24 GHz is proposed. Finally, a preliminary demonstrator for 2.4 GHz and our final demonstrator for 24 GHz are presented.

II. Multiband capable receiver architectures

Several different approaches to software configurable receiver architectures have been developed in the past. Of course, the performance of these receivers is mainly limited by the availability of active components and, thus, a reasonable compromise between flexibility, bandwidth, frequency of operation and expenses had to be found. Due to the technological constraints, the majority of software configurable receiver architectures in the literature are limited to a few discrete bands and/or the megahertz and lower gigahertz range [2]. Digitization of the IF as a reasonable intermediate step led to interesting solutions like a combined GSM/GPS receiver [3] or a multi-standard transceiver for UMTS, GSM, EDGE and BlueTooth [4].

The requirements for multiband receivers lead to two main needs regarding the receiver topology: On the one hand the center frequency has to be tuned over a large frequency range. On the other hand the bandwidths of the standards can differ by more than two decades. The limit of heterodyne receivers regarding the tunable bandwidth is given by the first IF frequency. Because of the non-linear character of the mixer, fourth order harmonics will arise between baseband and the double bandwidth of the input filter. This limits the maximum tuning bandwidth significantly or increases the number of IF stages up to an uneconomical number.

As an alternative to heterodyne receivers, the zero-IF or homodyne receiver topology uses a single mixing stage to convert the RF-signal to baseband [1]. In general, this approach requires I&Q down-conversion to preserve the information of both sidebands and, thus, two analog-to-digital-converters (ADC). Because the bandwidth of the standard determines the widths of the lowpass filters in front of the ADCs, reconfigurable or tunable filters are needed for multimode reception [5]. A leakage of the LO leads to partly time variant DC bias after the down converting process. This problem can partly be solved by using a very low IF implementing the conversion into the baseband in the digital domain [6].

Looking at mm-wave frequencies of operation the six-port receiver becomes attractive [7]. The six-port can be considered as a linear black box with two inputs and four outputs. The outputs are terminated by power detectors. The relations between input signals and the output signals can be derived by means of a calibration procedure. The feasible tuning bandwidth is given by the characteristics of the six-port itself and the subsequent power detectors. The channel bandwidth is defined by the lowpass filters behind the detectors.

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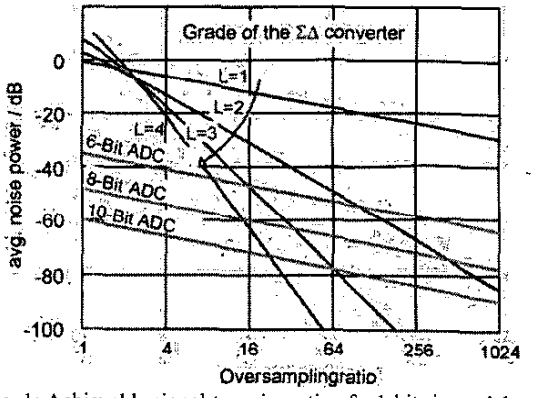

Fig. 1: Achievable signal-to-noise ratio of a 1-bit sigma delta converter and converters without noise shaping versus OSR

A straight-forward approach to software configurable receivers is to sample the input frequency itself. But at gigahertz frequencies, in particular at frequencies beyond 10 GHz, no direct digitization is feasible yet. A look at the roadmap of the development of commercial analog-to-digital-converters (ADC) shows clearly, that it can neither be expected in near future. Though applications in the microwave range usually use large absolute bandwidths of a few 100 MHz, the relative bandwidths are small, i.e. a few percent. Moreover, the interesting bands used by a certain class of applications (e.g. automotive radar, broadcast services, communication links) are widely separated. Thus, direct digitization would be very ineffective. In this case, band limited under-sampling can be used to reduce the sampling rate and the effort in processing the digital signals.

The well-known Nyquist criterion states that wide-band digitization of an RF-signal with a maximum frequency f requires a minimum sampling rate of $2 \cdot f$. But for a band-limited signal of bandwidth B the demands for the minimum sampling rate of the ADC relax to the value $2 \cdot B$ [8]. The key component of this architecture is the sample-and-hold (S/H) switch. The required bandwidth of this switch must be well above $2 \cdot f$. Moreover, the influence of sampling jitter and the requirements on the anti-aliasing filter increase when doing this [9]. Thus, only a moderate dynamic range can be expected in the microwave range.

Employing noise-forming sigma-delta ADC architecture even with a 1-bit-ADC a signal-to-noise ratio sufficient for many applications can be achieved [10]. In general, the sigma-delta bandpass ADC concept is capable of providing an impressing dynamic range by using a clocked 1-bit-ADC, a feedback loop and a loop filter, e.g. [11]. But perhaps the most critical parameter of this sampling concept is the timing jitter at the clocked components, in particular at the S/H-switch. Thus, the

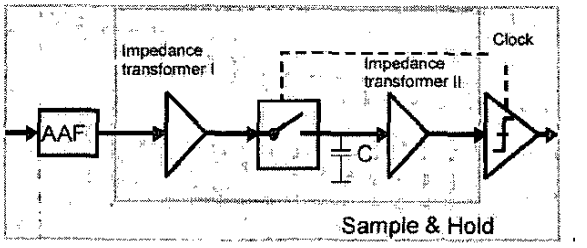

Fig. 2: Digital millimeter wave receiver architecture

feasibility of the whole concept is mainly determined by the feasibility of the S/H-switch. Highly linear switches were reported for sampling rates below 1 GS/s in CMOS technology [12]. In the range of several GS/s monolithically integrated diode bridges were used [13].

In order to achieve sample rates above 10 GS/s we employed a hybrid concept. On a monolithically integrated circuit (SiGe HBT) containing the buffer amplifiers we mounted Si Schottky diodes in flip-chip technology.

III. A Direct Sampling Receiver for 24 GHz

A. Concept

In case of band limited under-sampling the oversampling ratio (OSR) is defined as ratio of half the sampling rate related to the 3 dB-bandwidth of the filter. For an application in the ISM band (f_0 = 24 GHz) the required bandwidth would be B = 500 MHz. Assuming a ratio of

$$\frac{f_0 \cdot 4}{f_S} = n = 9 \qquad (1)$$

we obtain a sampling frequency of f_s=10.66 GHz and an OSR=10.66. The expected resolution of this ADC is 3 bit. By using a noise shaping sigma-delta-converter the resolution will be further improved [14] (Fig. 1).

Fig. 2 shows the architecture of the proposed digital millimeter wave receiver. The key components are the anti aliasing filter (AAF), the clocked S/H-circuit and the comparator (1-bit ADC). The AAF suppresses all out-of-band interferers in order to fulfill the Nyquist criterion at least regarding the bandwidth of the signal of interest.

The output voltage of the S/H-switch must track the input signal as long as the switch is closed. Thus, the output impedance of the first amplifier driving the switch has to be rather small. Good results are obtained for values of less then 10 Ω. Thus, an impedance transformer is needed to provide a 50 Ω port at the input of the circuit.

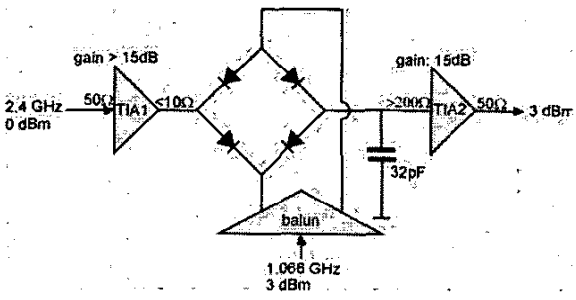

Fig. 3: Specification of the sampling head (for 2.4 GHz)

To keep the output voltage of the S/H switch constant as long as the switch is open, the input impedance of the second amplifier should be at least 200 Ω. So we need a second impedance transformer, to transform the 200 Ω impedance to the standard 50 Ω level of the subsequent stages. Moreover, both impedance transformers have to amplify the signals according to the dynamic range of the respective stages.

The key component of the receiver is the S/H-circuit as shown in the center of Fig. 3. As a sampling switch a silicon Schottky diode quadruple bridge is used, followed by a shunt lumped holding capacitor. The diodes are well suited because of their high reverse and their low forward resistance. As the diode switch contains four strong nonlinearities generating many harmonics and intermodulation products a precise simulation of the circuit is rather difficult but nonetheless absolutely essential. Generally spoken the diode switch is the most broad-banded component of the whole front-end.

To prevent cross talk between the incoming signal and the clock signal, the diode quadruple has to be driven symmetrically. This is achieved by implementing a balun circuit in the clock signal path.

B. Modeling

Our aim is the realization of the architecture shown in Fig. 2 for an input frequency of 24 GHz. As a first step, we designed, fabricated and characterized a scaled demonstrator for 2.4 GHz. Thus, we started from a specification of the sampling head as given in Fig. 3. The impedance, power and gain levels were chosen according to the prospective feasibility in the 24 GHz target system.

For the simulation we used a harmonic balance approach. We employed silicon Schottky diodes from DaimlerChrysler. The diode parameters were extracted from DC and RF measurements. For our first 2.4 GHz demonstrator a hybrid chip capacitor was used as a holding capacitor. Measurements showed that the parasitic inductances of the bonding wires and via holes that were

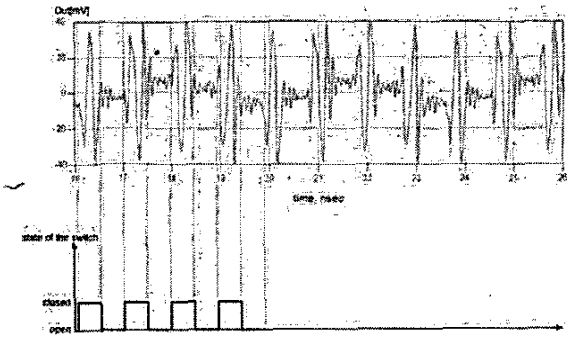

Fig. 4: Simulated voltage across the holding capacitor

neglected during the design of the circuit resulted in unacceptable oscillations during the "hold" phase. Thus, in a second design, this capacitor was integrated monolithically.

Fig. 4 shows the simulated results (after inclusion of the parasitic inductances), namely the voltage across the holding capacitor in time domain. As can be seen, during the "closed" ("track") phase the voltage tracks the 2.4 GHz input signal. During the "open" ("hold") phase, the voltage is held. But some high frequency oscillations can be observed during the "hold" phase. This problem could be solved by monolithic integration of the holding capacitor. In this case, the voltage is almost perfectly flat during the "hold" phase.

C. Demonstrator for 2.4 GHz

A demonstrator was built according to the specifications given in Fig. 3 and characterized. Both impedance transformers were designed by University of Ulm and realized by ATMEL in Si/SiGe technology. They were assembled on one chip where the diodes were flip-chip bonded onto. Fig. 5 shows a photo of the first realization of the sampling head. On the right hand side the chip holding capacitor connected by a bond wire can be seen. Our second design is almost identical with the exception of the monolithically integrated holding capacitor.

Measured results were very similar to the simulated ones. This demonstrates that our models as well as the used methods are appropriate and will probably correctly predict the behavior of the target system at 24 GHz.

D. Demonstrator for 24 GHz

Since simulations at 24 GHz led to reasonable results, we used the specifications given in Fig. 3. Only the holding capacitor was adapted to 3.2 pF.

Fig. 6 shows the readily assembled 24 GHz front-end chip. Again, the design of the impedance transformers was done at University of Ulm. The chip was fabricated by

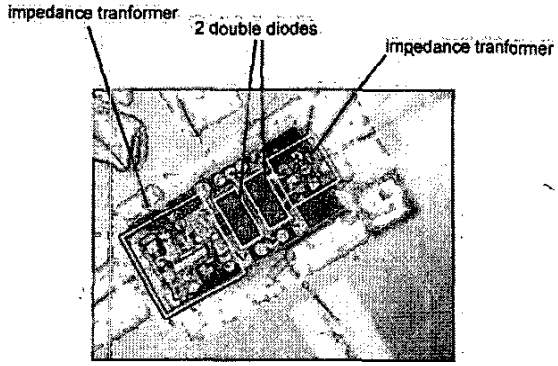

Fig. 5: 2.4 GHz sampling head

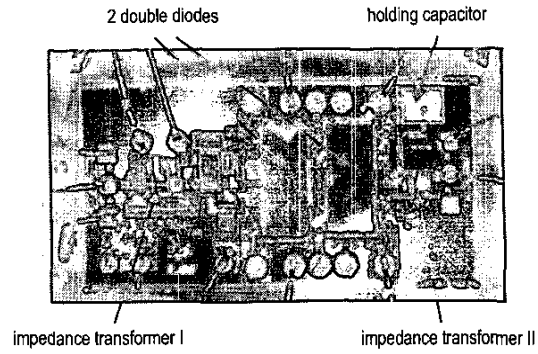

Fig. 6: 24 GHz sampling head

ATMEL in Si/SiGe technology. The diodes fabricated by DaimlerChrysler were mounted in flip-chip technology. First measurements showed that all components work properly. No quantitative experimental results have been obtained yet, but will be presented at the conference.

IV. Conclusion

The direct sampling receiver based on band-limited under-sampling is a flexible solution suited for millimeter wave frequencies, but it is a very ambitious approach. It still needs extensive development, but first results are very promising. The critical components have been analyzed and specified. Functionality at 2.4 GHz could be proven and a first working 24 GHz front-end was fabricated.

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